ANTIFUSE OPTION FOR ROW REPAIR

This application is a Continuation of U.S. Application No. 10/008,409, filed November 13, 2001, which is a Divisional of U.S. Application No. 09/005,815, filed January 12, 1998, now U.S. Patent No. 6,317,370.

Field of the Invention

The present invention relates to semiconductor based memory devices, and in particular to controlling timing in a dynamic random access memory (DRAM) based on row repair.

Background of the Invention

Semiconductor memory devices are becoming more and more complex as their size decreases and their storage density increases. To help handle some of the increase in storage density, an architecture comprising multiple subarrays of memory cells on a die for storing values such as bits has been adopted in dynamic random access memory (DRAM) devices. Each of the subarrays comprises multiple rows of memory cells that are accessed or "fired" by activation of row address signals. Occasionally, during manufacture, one or more rows is defective. Some of these rows may be replaced via a fuse option with redundant rows such as shown in US Patent No. 5,528,539 to Ong et. al. When a redundant row is used, the DRAM's internal timing needs to be slightly slowed down, to provide extra time for address compare and override to the redundant rows. Repair of DRAMs during manufacturing happens on a manageably small percentage of parts, often less than 50%. Therefore, it is not desirable to slow down every die regardless of row repair. In fact, it is desired to obtain faster row access speeds if possible.

Prior solutions have included providing circuits on the die that poll every redundant row bank on the die. If any are enabled, the RAS chain is slowed down.

Such schemes, while easy to implement on smaller generation DRAMs, mandate a large number of line spaces and gates for the polling operation on higher density generation DRAMS, since there may be 16 to 64 row banks or more that are checked. This consumes valuable die space and adversely impacts efforts to further increase DRAM

5   density.

There is a need for slowing down the RAS chain when redundant rows are used. There is a further need to only slow down the RAS chain when such redundant rows are in use. There is a need to slow down the RAS chain without using significant additional circuitry. In fact, it would be beneficial to reduce the amount of circuitry currently used

10   to determine that the RAS chain needs to be slowed down.

Summary of the Invention

A fuse option is provided in a memory device to selectively slow row address signals when redundant rows of memory cells have been selected for use. The fuse

15   option is blown when a redundant row is used to replace a defective row as identified during manufacture of a chip. Use of the fuse allows removal of multiple lines and gates used to poll row banks to determine if a redundant row was in use. The removal of such lines and gates creates more room for other circuitry, contributing to the ability to create higher density memory devices.

20   In one embodiment, a fuse is coupled to delay circuitry which has a known delay. When the fuse is blown after detecting a defective row, the delay circuitry is coupled in series with selected portions of a row address strobe (RAS) chain of circuitry used to propagate row address selection signals to the proper rows. This provides extra time needed for row address compare and override circuitry, which is not in series with

25   the delay circuitry.

In a further embodiment, an antifuse takes the place of the fuse and is coupled such that when it is set, the delay circuitry is appropriately coupled into the path of selected portions of the RAS chain. The present invention is useful in the design and manufacture of dynamic random access memory (DRAM) devices.

Brief Description of the Drawings

Figure 1 is a logic schematic diagram of a prior art polling technique for fast/slow RAS chain control.

Figure 2 is a block diagram of dynamic random access memory (DRAM) device with a fuse option to control the fast/slow RAS chain.

Figure 3 is a detailed block diagram of the fuse option for fast/slow RAS chain control of Figure 2.

Figure 4 illustrates a computer in which the present invention may be used.

Figure 5 illustrates a block diagram of an interface for a microprocessor and a memory device of Figure 2.

Description of the Embodiments

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention. The terms wafer and substrate used in the following description include any semiconductor-based structure having an exposed surface with which to form the integrated circuit structure of the invention. Wafer and substrate are used interchangeably to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

Figure 1 is a prior art drawing of a logic level schematic showing how the RAS chain is typically slowed down based upon the polling of every redundant row fuse bank on the die. Fuse bank 50A corresponds to the fuse bank for a memory subarray which controls whether redundant rows have been used to replace a defective row of the

5 memory sub array. A plurality of fuse banks such as 50A, 50B, 50C,..., 50N, may be found for a dense memory array comprised of N sub arrays. The fuses are polled by a polling network of combinational logic 52, shown in Figure 1. The result of the combinational logic is a single signal 54 which corresponds to a fast or slow control signal. This signal controls the RAS chain to instruct the RAS chain to either go fast in

10 the case of no redundant rows being substituted for defective rows, or slow if any one row had been replaced with a redundant row. The fuses of fuse banks 50A...50N may be fuses, anti-fuses, laser fuses and the like. The slowing of the RAS chain is to compensate for the increased time required for address matching and override in the case of the use of a redundant substituted row. Those skilled in the art will readily

15 recognize that the type of fuses used in the fuse bank will effect the type of combinational logic 52 required to produce the appropriate fast slow signal 54.

Figure 2 is a block diagram of an illustrative embodiment of the present invention. A DRAM 100 includes a memory array 102 formed on a semiconductor substrate. Multiple DRAMs are formed on the same substrate, each one being separated

20 at some point late in the manufacturing process to form an integrated circuit known as a memory chip. Memory array 102 includes rows and columns of addressable memory cells. Each memory cell in a row is coupled to a common word line. Additionally, each memory cell in a column is coupled to a common bit line. Each cell in memory array 102 includes a storage capacitor and an access transistor as is conventional in the art.

25 DRAM 100 interfaces with, for example, microprocessor 104 through address lines 117 and data lines 116. Alternatively, DRAM 100 may interface with a DRAM controller, a microcontroller, a chip set or other electronic system. Microprocessor 104 also provides a number of control signals to DRAM 100, including but not limited to,

row and column address strobe signals RAS* and CAS*, write enable signal WE*, an output enable signal OE* and other conventional control signals.

Row address buffer 108 and row decoder 110 receive and decode row addresses from row address signals provided on address lines 117 by microprocessor 104. Each unique row address corresponds to a row of cells in memory array 102. Row decoder 110 includes a word line driver, an address decoder tree, and circuitry which translates a given row address received from row address buffers 108 and selectively activates the appropriate word line of memory array 102 via the word line drivers. Further, when defective rows have been discovered during a probe test at the wafer level while the chip is being manufactured, the unique row address is remapped to a spare row, usually by use of a settable fuse in a row of fuse banks 120 coupled to or within row decoder 110. When remapped, the path to decode the address is longer, and it takes more time for the address to be ready from the row decoder 110.

Column address buffer 112 and column decoder 114 receive and decode column address signals provided on address lines 117. Column decoder 114 also determines when a column is defective and the address of a replacement column. Column decoder 114 is coupled to sense amplifiers 105. Sense amplifiers 105 are coupled to complementary pairs of bit lines of memory array 102. Sense amplifiers 105 include equilibration circuits that bias the complementary bit lines at a selected voltage prior to reading data from a cell of memory array 102. Advantageously, the equilibration circuits are controllably coupled to a reference voltage supply such that the reference voltage supply may be decoupled from the equilibration circuit to prevent current leakage due to a defective column.

Sense amplifiers 105 are coupled to data-in buffer 107 and data-out buffer 106. Data-in buffers 107 and data-out buffers 106 are coupled to data lines 116.

During a write operation, data lines 116 provide data to data-in buffer 107. Sense amplifier 105 receives data from data-in buffer 107 and stores the data in memory array 102 as a charge on a capacitor of a cell at an address specified on address lines 117.

During a read operation, DRAM 100 transfers data to microprocessor 104 from memory array 102. Complementary bit lines for the accessed cell are equilibrated during a precharge operation to a reference voltage provided by an equilibration circuit and a reference voltage supply. The charge stored in the accessed cell is then shared

5   with the associated bit lines. A sense amplifier of sense amplifiers 105 detects and amplifies a difference in voltage between the complementary bit lines. The sense amplifier passes the amplified voltage to data-out buffer 106.

Advantageously, the reference voltage supply used to equilibrate the bit line in this embodiment may be selectively decoupled from the equilibration circuit using a

10   gating transistor to prevent leakage current due to a defective bit line. This can be accomplished using, for example, a modified column select signal which turns off a transistor coupled between the equilibration circuit and the reference power supply.

Control logic 118 is used to control the many available functions of DRAM 100. It receives address strobe signals from microprocessor 104 and uses them to control the

15   timing of the operation of DRAM 100 as well as the transfer of data to and from microprocessor 104. In prior systems, the control logic 118 received a fast/slow signal from a series of NAND gates coupled by conductive lines to the row fuse banks. When one of the fuses in the fuse banks was set due to the need to replace a defective row of memory, the fast/slow signal was active, indicating that control logic 118 should slow

20   down the RAS* signal at some point in the circuitry carrying the RAS* signal, referred to as the RAS chain, in order to allow more time for the redirection to the redundant row. The RAS* signal is slowed by approximately 2-3 nanoseconds in one embodiment by the simple insertion of well known delay elements in the RAS chain. The high number of redundant rows in higher density DRAM devices lead to larger numbers of

25   conductive lines and NAND and NOR gates to accomplish the slow down. This required much chip real estate, decreasing the area available for memory circuitry.

To greatly reduce the real estate required for accomplishing the slow down, a settable fuse 122 is coupled to control logic 118. The settable fuse comprises one of many types of fuses, including an antifuse or a fuse or any other type of element which

can be used to modify current paths. An antifuse operates as a short circuit when fabricated. By applying a large voltage to the antifuse structure, the antifuse becomes "programmed." A programmed antifuse, fabricated as well known to one skilled in the art, operates as a conductor or link in a closed circuit, allowing current to flow through

5   that part of the circuit. In comparison, a fuse operates as a link in a closed circuit when fabricated. The fuse is fabricated and selectively melted by methods well known to one skilled in the art, such as by an electric current, overvoltage or laser. Once the fuse is melted, it operates as an open circuit. Either type of fuse may be used, and in one embodiment, it is the same type of fuse as is used in fuse bank 120.

10   In a further embodiment, the fuse 122 is located adjacent to, or in the fuse bank 120 and is coupled by a conductive line to control logic 118 to accomplish the same slow down. This greatly simplifies the circuitry required to accomplish the slow down, and since a fuse is being set for substituting a different row of memory cells, the fuse 122 may be set at the same time, either before, after or simultaneously with the row

15   substitution fuse without having to reposition equipment to set the fuse to a different area of the chip. It is very easy to simply blow one more fuse once a fuse must be blown for use of a redundant row.

           In yet a further embodiment, fuse 122 is already set in a condition to slow down the RAS chain, and is set when no redundant rows are used such that the RAS chain

20   operates in a fast mode, and data is made available more quickly to the microprocessor 104 just as in the first embodiment, where the fuse is set only when a redundant row is used. Fuses are used, as they may be set late in the manufacturing process, after rows are operable and testable. By only slowing down the RAS chain when a substitute row is actually used, memory chips not using spare rows may be allowed to operate at a

25   higher speed. This provides a higher yield of faster parts when speed graded to approximately 10 nanosecond deltas.

           Several other control circuits and signals not detailed herein initiate and synchronize DRAM 100 operation as well known to those skilled in the art. As stated above, the description of DRAM 100 has been simplified for purposes of illustrating the

present invention and is not intended to be a complete description of all the features of a DRAM. Those skilled in the art will recognize that a wide variety of memory devices, including but not limited to, SDRAMs, SLDRAMs, RDRAMs and other DRAMs and SRAMs, VRAMs and EEPROMs, may be used in the implementation of the present

5   invention. The DRAM implementation described herein is illustrative only and not intended to be exclusive or limiting.

Figure 3 shows a detail of the fast slow signal 154 as used to create a fast or slow RAS chain operation. The entire combinational logic tree used to poll the plurality of fuses in the plurality of fuse banks is replaced, in the preferred embodiment, by a

10   signal fuse 122. At the time of testing and replacement of defective rows with redundant rows, the redundant row fuse is programed and the fast slow fuse 122 is also programmed. The elimination of the combinational logic tree 52, saves a large amount of die area in the memory 100. Those skilled in the art will readily recognize that the type of fuse used in the fuse 122 may be of a wide variety, as described above.

15   A personal computer is shown in Figure 4 which includes a monitor 400, a keyboard input device 402 and a central processing unit 404. The processor unit typically includes microprocessor 104, memory bus circuit 408 having a plurality of memory slots which accept DRAM memory chips 100(a-n), and other peripheral circuitry 410. Peripheral circuitry 410 permits various peripheral devices 424 to

20   interface processor-memory bus 420 over input/output (I/O) bus 422.

Coupled to memory bus 420 are a plurality of memory slots which receive memory devices 100(a-n) . For example, single in-line memory modules (SIMMs) and dual in-line memory modules (DIMMs) may be used in the implementation which utilize the teachings of the present invention. Each type of integrated memory device

25   has an associated communications speed which in turn limits the speed data can be read out of or written into memory bus circuit 408.

These memory devices can be produced in a variety of designs which provide different methods of reading from and writing to the dynamic memory cells of memory 112. One such method is the page mode operation. Page mode operations in a DRAM

are defined by the method of accessing a row of a memory cell arrays and randomly accessing different columns of the array. Data stored at the row and column intersection can be read and output while that column is accessed. Page mode DRAMs require access steps which limit the communication speed of memory circuit 408. A typical communication speed using page mode a DRAM device is approximately 33 MHZ.

An alternate type of device is the extended data output (EDO) memory which allows data stored at a memory array address to be available as output after the addressed column has been closed. This memory can increase some communication speeds by allowing shorter access signals without reducing the time in which memory output data is available on memory bus 420. Other alternative types of devices include SDRAM, DDR SDRAM, SLDRAM and Direct RDRAM as well as others such as SRAM or Flash memories.

CONCLUSION

It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description. As previously mentioned, the use of fuses and antifuses are one design choice, as well as the location of the fuses, and various methods of setting the fuses are well within the scope of the invention. Further, it is well known that DRAM devices are comprised of multiple subarrays, each subarrary having corresponding redundant rows, or a bank of redundant rows being provided for all the subarrays. The sizes and numbers of subarrays can also be varied without departing from the invention. Still further, other types of memory devices making use of redundant rows of memory selectable by whatever method may make use of the present invention.